Specification Amendments

Amend the Title as follows:

TEST STRUCTURE ~~AND METHOD~~ FOR DETERMING A MINIMUM TUNNEL OPENING SIZE IN A NON-VOLATILE MEMORY

Amend the Abstract as follows:

~~A test structure is disclosed for determining the smallest acceptable tunnel size in a non-volatile memory cell. Additionally, defect density for one or more tunnel opening sizes may also be determined. In one aspect, the test structure has continuous strips of active area that are used to form a "control" path, a "read" path, and a "write" path. A dielectric layer is formed over the active strips. A one-dimensional array containing a number (N) of same-sized tunnel openings is formed on the write path. A layer of polysilicon is deposited over the dielectric and patterned into strips that are perpendicular to the active strips. The polysilicon strips are aligned with the tunnel openings and form a floating gate and sense device, which is capacitively coupled to external probe pads through the common "control" path. The test structure may have a series of write paths wherein a write path has a one-dimensional array of "N" same-size tunnel openings. The first write path typically includes an array of tunnel openings with a relatively large size, with each additional write path containing an array of tunnel openings of incrementally descending size. The test structure allows bulk (all N gate simultaneously) programming or erasing of any one-dimensional array of a tunnel opening size. Consequently, a large number of same-size tunnel openings may be tested in parallel.~~

In one embodiment of the invention, a test structure for testing the sufficiency of tunnel opening sizes in a non-volatile memory cell includes N write paths aligned substantially in parallel, each of the write paths beings individually programmable and M floating gates, each of the floating gates overlapping each of the multiple write paths to form a N column-by-M row array of intersecting areas. An N

column-by-M row array of tunnel openings is formed in the intersecting areas and between the floating gates and write paths, with the tunnel openings in each array column being of a same size and the tunnel openings in each array row being of different sizes. A read path coupled to the M floating gates is operable to detect a programmed write path if the tunnel openings formed over the programmed write path are of sufficient size to successfully couple the M floating gates to the programmed write path.